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Design of Semi-Static SET Flip-Flop for Low Power and High Performance Applications

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***Abstract*— The paper proposed a new design for implementing semi-static flip-flop for low power and high performance applications. In this work, comparative analysis of six existing flip-flop designs along with the proposed design is made. The proposed design has better power, delay and PDP than the existing architectures. All simulations are performed on TSpice using BSIM models in 130 nm process node. The simulation results show that for all supply voltages, all clock frequencies and all data activities, the proposed flip-flop has the better power consumption than all the six existing flip-flops discussed in this paper. The proposed flip-flop also shows the second lowest PDP and the second shortest delay.**

***Keywords*— Single edge triggered, PDP, Energy efficient, High performance**

I. INTRODUCTION

In CMOS digital logic design, power consumption has been a major concern for the past several years. Due to the advancement in IC fabrication technology that allows the use of nano-scale devices, the power dissipation is a prominent issue [1]. In the present design consideration the power consumption and chip area requirements are small and the operating frequency is high compared to conventional discrete I.C. design, so low power design with high performance is becoming increasingly important [2]**.** Flip-flops are widely used in building many sequential logic circuits such as registers, memory elements, counters, etc. These circuits are heavily used in the implementation of VLSI chips. Therefore the improvement in power consumption of such circuits, without weakening other characteristics, is of prime importance to the VLSI industry [3].

In this paper, a new architecture of single edge triggered flip-flop is proposed. The conventional and the proposed single edge triggered flip-flop are presented and compared. The superior performance of the proposed work has been pointed out, providing high frequencies across supply voltages. For all circuits, simulations are carried on 130nm process node using BSIM3 models.

This paper is organized into six sections. Section II compares the existing single edge triggered flip-flop structures. In section III, a new flip-flop structure is proposed. The nominal simulation conditions, along with analysis and optimization performed during simulation, are discussed in section IV. In section V results are presented and proposed design is compared with conventional designs in terms of power, delay, PDP and transistor count. Section VI ends the paper with conclusion.

II. EXISTING SINGLE EDGE TRIGGERED FLIP-FLOPS

The static Push Pull Flip-Flop (PPFF) is shown in Fig. 2. To improve the performance of a conventional Transmission Gate Flip-Flop (TGFF shown in Fig. 1) [4], [5], addition of an inverter and transmission gate between the outputs of master and slave latches to accomplish a push–pull effect at the slave latch, was proposed in [6]. This increased 4 transistors. To compensate this increment of transistor count, two transmission gates are eliminated in the Push Pull Flip-Flop from the feedback paths of conventional TGFF.

Fig. 3 shows the static C^2MOS Flip- Flop [7]. This flip-flop consists of a C^2MOS feedback at the outputs of the master and the slave latches. When clock is at logic 'HIGH', the clocked inverter CLKI1 latches the input D to an intermediate node N. The feedback consisting of clocked inverter CLKI2 and inverter I1 maintains this logic level at node N when clock is at logic level 'HIGH'. Similarly when CLK changes to logic 'LOW', the slave latch gets functional and clocked inverter CLKI3 transfers the logic level from node N to the output Q. The feedback consisting of clocked inverter CLKI4 and inverter I2 maintains this logic level at output node Q when clock is grounded. There are 20 transistors in this circuit. So C^2MOSFF has largest area but this flip-flop shows the shortest delay and the lowest PDP.

The Area Efficient flip-flop was proposed in [8]. This semi-static flip-flop is illustrated in Fig. 4. This flip-flop has lesser transistor count as compared to above discussed flip-flops. In this design the feedback circuit of the master section is removed and in slave section, feedback loop consists of a transmission gate. When clock level is 'HIGH', master latch is functional and inverse of the data is stored to an intermediate node N. When clock goes to 'LOW' logic level, the slave latch becomes functional and produces data at the output Q and QB.

In High Performance Flip-Flop (HPFF)**,** a feedback is provided from the output node of the slave inverter to a specific internal node in the master-stage as shown in Fig. 5. This flip-flop was proposed by [9]. This feedback is provided by only a single transistor. So this has lesser number of transistor as compare to other flip flops. The main advantage of this design is reduced device count and decreased parasitic capacitance at internal nodes of the flip flop which results in improved power-delay product.

To save power, the number of transistors of the proposed flip-flop was reduced in [10]. The four transistors in the feedback path of conventional TGFF are replaced by single PMOS transistor. Hence, total 6 transistors are reduced

in this flip-flop. This semi-static Pass Flip-Flop (Pass FF) is shown in Fig. 6.

To activate the feedback path of pass FF only during OFF cycle, a PMOS transistor was added in the feedback in [10]. This semi-static Pass Isolation Flip-Flop (PIFF) is shown in Fig. 7. As compare to Pass FF, the number of transistors of this flip-flop is increased by two but this reduces short circuit current during ON cycle. It also improves speed as compare to Pass FF.

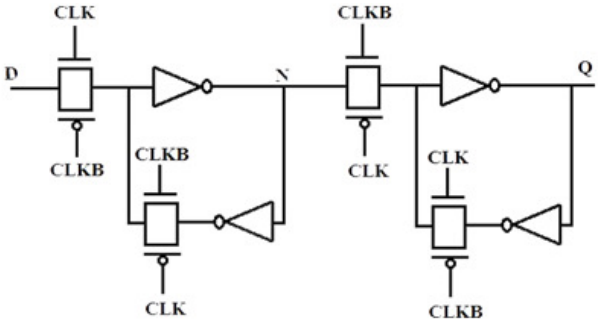

Fig. 1 Conventional Transmission Gate Flip-Flop (TGFF)

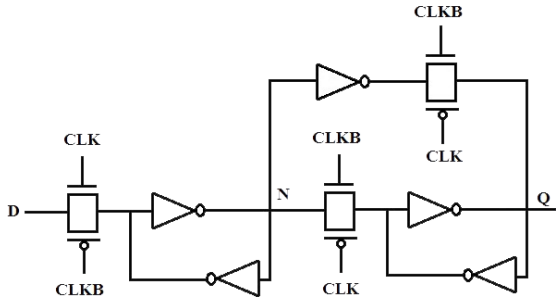

Fig. 2 Push Pull Flip-Flop (PPFF)

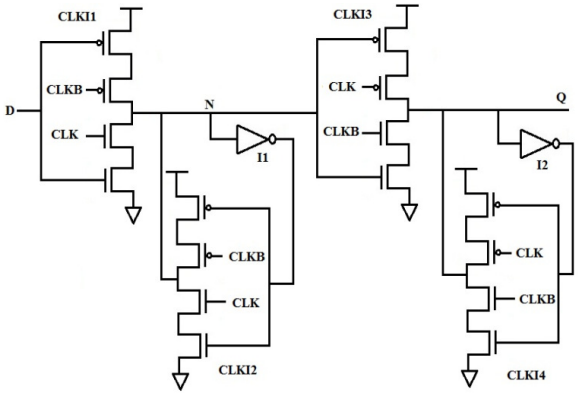

Fig. 3 C^2MOS Flip-Flop (C^2MOS FF)

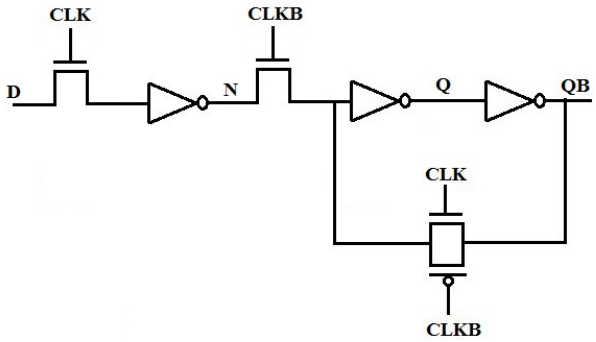

Fig. 4 Area Efficient Flip-Flop (Area Efficient FF)

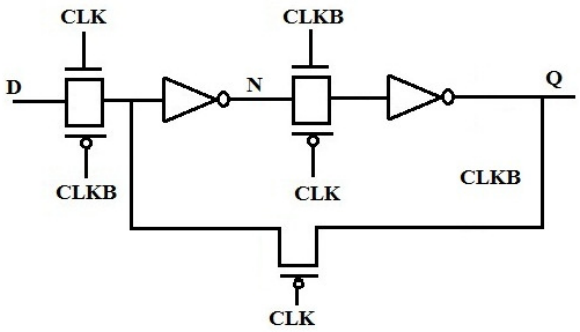

Fig. 5 High Performance Flip-Flop (HPFF)

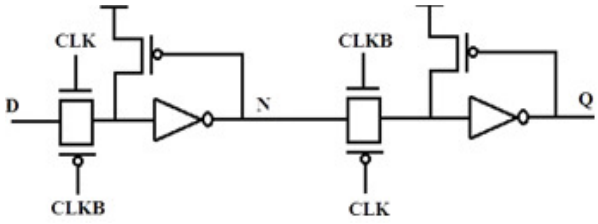

Fig. 6 Pass Flip-Flop (Pass FF)

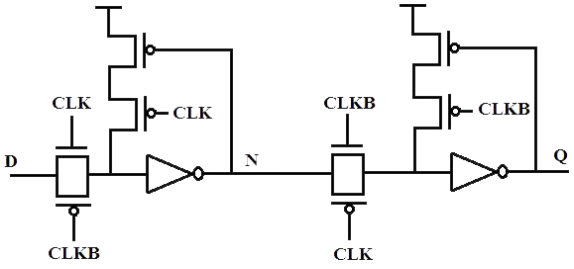

Fig. 7 Pass Isolation Flip-Flop (PIFF)

III. Proposed SET Flip-Flop for Low Power and High Performance Applications

The new SET flip-flop structure is proposed in this paper. The proposed flip-flop (proposed FF) is shown in Fig. 8. To make the proposed flip-flop semi-static in nature, two PMOS transistors are used in series for the weak pull up in both master and slave latches. One of these transistors is grounded,

so this transistor is permanently ON to reduce the switched capacitance. This improves the power efficiency of the proposed flip-flop. The flip-flop is the modification of PIFF. In the proposed FF when clock level is 'HIGH', master latch is activated and inverse of the data is stored to an intermediate node N. When clock goes to 'LOW' logic level, slave latch becomes functional and produces data at the output Q. There are twelve transistors in this flip-flop, in which four are clocked transistors. This flip-flop has low area. The main advantage of the proposed design is lesser power consumption, delay and PDP without using the large number of transistors.

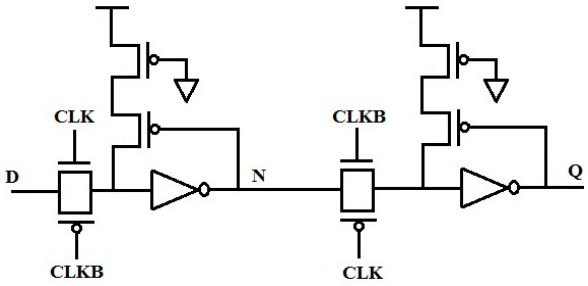

Fig. 8 Proposed Flip-Flop (Proposed FF)

IV. SIMULATION

Simulation parameters used for comparison, are shown in table 1. Under nominal condition, a 16-cycle sequence (1111010110010000) with an activity factor of 50% is supplied at the input for average power measurements. Different data patterns should be applied with different activity rates to obtain a fair idea of power dissipation for a circuit topology [11]. So in simulations, five different data sequences have been adopted to compare the power consumption of flip-flop structures discussed in this paper.

The results are carried out for the period of 16 data sequences. All simulations are performed on TSpice using BSIM 3v3 level 53 models in 130 nm process node. The supply voltage is varied from 1V to 2V. The clock frequency is varied from 100MHz to 1GHz.

A. Analysis

The flip-flops can be compared for various parameters. For example we can compare delay, power consumption, power delay product (PDP), energy delay product (EDP), energy delay squared product (ED^2P) and latency of flip-flops [12]. In this paper, our main interest is in SET FF usage for low-power applications. Therefore power consumption is selected for comparing different flip-flops. Additionally Delay and PDP are also compared of the discussed flip flops.

B. Optimization

There is always a trade-off between power dissipation and propagation delay of a circuit. A flip-flop can be optimized for either high performance or low power, but both the parameters are critical. In this work, the designs are simulated to achieve minimum power dissipation.

The feedback path is improved in the proposed flip-flop. In the proposed flip-flop, two PMOS transistors are used in series for the weak pull-up to provide a feedback. One of these transistors is grounded, so this transistor is permanently ON to reduce the switched capacitance. This improved the power efficiency of the proposed flip-flop. The proposed flip-flop is negative edge triggered. The proposed flip-flop is semi-static in nature. The transistors, that are not located on critical path, are implemented with minimum size to reduce area overhead and to minimize power dissipation.

V. RESULT AND DISCUSSION

Table II shows the power consumption in microwatts at different supply voltages for 50% data activity and 400MHz clock frequency. The simulation results indicate that the proposed FF has the least power dissipation among all the designs for all supply voltages. For fair comparison, the average of power consumption at all voltages is taken except 1V, because at 1V two previously proposed flip-flops failed. This result shows that the proposed FF has 45.95%, 48.16%, 52.32%, 33.78%, 40.12% and 50.80% improvement in average power consumption when compared to the previously proposed flip-flops discussed in section 2 respectively. Proposed FF has up to 52.32% improvement in average power consumption. From 1V to 1.4V C^2MOSFF consumes highest power while for 1.6V PIFF consumes highest power. For 1.8V and 2V Area efficient FF shows the highest power consumption. PPFF and Area efficient FF failed at 1V. Among previously proposed flip-flops discussed in section 2, HPFF shows the lowest power consumption.

Table III shows power consumption in microwatts as a function of clock frequency. Table shows that for all clock frequencies, the proposed FF has the lesser power consumption than all the existing flip-flops. For fair comparison, the average of power consumption at all clock frequencies is taken. This average result shows that the proposed FF consumes 41.24%, 46.51%, 33.61%, 35.60%, 40.81% and 46.06 lesser average power as compared to the previously proposed flip-flops. Among previously proposed flip-flops discussed in section 2, HPFF has lesser power consumption at all clock frequencies except 400MHz and 1 GHz, at these frequencies AEFF and PPFF consumes lesser power respectively. For 100MHz and 200MHz clock frequencies, PIFF has the highest power consumption. At 250MHz PPFF consumes the highest power while for 400MH and 1 GHz C^2MOSFF shows the highest power consumption.

Power Consumption in µW as a function of data activity is shown in table IV. The proposed FF shows the best power performance for all switching activities. Among previously proposed flip-flops discussed in section 2, PPFF consumes the lowest power for 0% (all 1's) data activity and AEFF consumes the lowest power for all data activity except 0% (all 1's). C^2MOSFF has the highest power consumption

for all data activities. For fair comparison, the average of power consumption at all data activities is taken. This average result shows that the proposed FF has 39.73%, 47.34%, 31.09%, 36.73%, 39.50% and 42.88% improvement in average power consumption when compared to the previously proposed flip-flops discussed in section 2 respectively.

Table V shows average clock to output (C_Q) delay in pS at different supply voltages for 50% (1111010110010000) data activity and 400MHz clock frequency. The simulation results indicate that the proposed FF has the shortest delay among all the designs for 1.6V and 1.8V supply voltages, the second shortest delay for 1.2V and the third shortest delay for 1V, 1.3V and 2V. C^2MOSFF shows the shortest delay for all supply voltages except 1.6V and 1.8V, at these two voltages the proposed FF has the shortest delay. For fair comparison, the average of delay at all voltages is taken. This result shows that the proposed FF has 59.01%, 77.80%, 20.18%, 49.64% and 27.46% improvement in average delay when compared to the previously proposed flip-flops discussed in section 2 respectively except C^2MOSFF. Proposed FF has up to 77.80% improvement in average delay. C^2MOSFF shows 57.65% lesser average delay when compared to the proposed FF. The simulation results indicate that for 1V supply voltage HPFF shows the longest delay and for 1.2V, 1.3V, and 1.4V Area Efficient FF has the longest delay. As supply voltage increases, delay of PPFF increases as compared to other flip-flops and for 1.6V, 1.8V, 2V this flip-flop shows the longest delay. Overall the average result shows that Area Efficient FF has the longest delay.

Table VI shows the clock to Q PDP as a function of supply voltage. For 1.6V and 1.8V supply voltages the proposed FF shows the lowest PDP while for 1.0V, 1.2V, 1.3V, 1.4V, and 2.0V it shows the second lowest PDP. For 1V, 1.2V, 1.3V, 1.4V and 2.0V C^2MOSFF shows the lowest PDP while for 1.6V and 1.8V it shows the second lowest PDP. For fair comparison, the average of PDP at all voltages is taken except 1V, because at 1V two existing flip-flops failed. This average result shows that the proposed FF has 81.08%, 84.96%, 48.70%, 73.18% and 68.59% improvement in PDP when compared to the previously proposed flip-flops discussed in section 2 respectively except C^2MOSFF, it has 17.90% lower PDP than the proposed FF. At 1V Pass FF has highest PDP. For 1.2V, 1.3V, 1.4V AEFF has highest PDP while for 1.6V, 1.8V and 2V PPFF shows the highest PDP.

Table 7 illustrates the transistor count for the various flip-flop designs discussed in this paper. The proposed design is composed of twelve transistors and has four clocked transistors which are equal to the lowest number of clocked transistors among all the previously proposed flip-flops discussed in section 2. Proposed FF has two more transistors than Area efficient FF, Pass FF and three more transistors than HPFF but table II, table V and table VI shows that proposed FF has lesser power, delay and PDP over these flip-flops respectively.

VI. CONCLUSIONS

A comparative analysis of single input single edge triggered flip-flops has been done. PPFF and Area efficient FF failed at 1V power supply. C^2MOSFF has largest transistor count, so where area is of prime concern, C^2MOSFF should not be used but C^2MOSFF shows the lowest delay and PDP, so it is suited for high performance applications where power and area are not at high priority. Area efficient FF has only ten transistors but this flip-flop has the longest delay and the highest PDP. So the Area efficient FF is not suited for high performance applications.

The new flip-flop structure has been proposed in this paper. The proposed flip-flop structure is compared on the basis of power, delay, PDP and transistor count with the existing flip-flop structures. For all supply voltages, all clock frequencies and all data activities, the proposed FF has the better power consumption than the existing flip-flops. The simulation results indicate that the Proposed FF has up to 52.32% improvement in average power consumption. Proposed FF shows the second lowest PDP having up to 84.96% improvement in PDP and the second shortest delay having up to 77.80% improvement in delay. So, proposed FF is best suited for low power and high performance applications.

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Table I CMOS Simulation Parameters

S. No.	1	2	3	4	5	6	7	8	9	10	11
Particulars	CMOS Technology	Min. Gate Width	Max. Gate Width	MOSFET Model	Nominal Supply Voltage	Temperature	Duty Cycle	Nominal Clock Frequency	Sequence Length	Rise Time of Clock & Data	Fall Time of Clock & Data
Value	130 nm	260 nm	1.44 µm	BSIM 3v3 level 53	1.3V	25° C	50 %	400MHz	16 Data Cycles	100 ps	100 ps

Table II Power consumption in µW as a function of supply voltage

VDD (V)	PPFF	C^2MOSFF	AEFF	HPFF	Pass FF	PIFF	Proposed FF
1.0	Failed	3.90	Failed	3.10	3.23	3.28	2.16
1.2	4.80	5.40	3.83	4.60	4.70	4.97	2.86
1.3	5.65	6.30	5	5.24	5.52	5.94	3.37
1.4	6.50	7.40	6.31	6.00	6.40	7.34	4.06
1.6	10.10	10.10	9.67	7.90	8.40	10.90	5.14
1.8	12.40	12.90	15.05	9.50	10.70	13.64	6.52
2.0	15.40	15.10	22.3	11.50	13.80	17.42	7.69
Average (excluding 1V)	9.14	9.53	10.36	7.46	8.25	10.04	4.94

Table III Power consumption in µW as a function of clock frequency

Clock Frequency (MHz)	PPFF	C^2MOSFF	AEFF	HPFF	Pass FF	PIFF	Proposed FF
100	3.50	3.00	2.97	2.50	3.10	3.63	1.70
200	4.20	4.00	3.66	3.30	4.00	5.01	2.21
250	4.50	4.40	4.01	3.80	4.20	4.25	2.40
400	5.70	6.30	5.00	5.20	5.50	5.94	3.37
10000	9.50	12.40	8.61	10.20	10.40	11.00	6.40
Average	5.48	6.02	4.85	5.00	5.44	5.97	3.22

Table IV Power Consumption in µW as a function of data activity

Data Activity (Data Pattern)	PPFF	C^2MOSFF	AEFF	HPFF	Pass FF	PIFF	Proposed FF
0% (1111111111111111)	3.30	4.30	4.2	4.00	3.60	3.80	2.34
0% (0000000000000000)	3.20	4.80	2.58	4.00	3.50	3.64	2.48
50% (1111010110010000)	5.70	6.30	5.00	5.24	5.50	5.94	3.37
50% (1100110011001100)	5.70	6.30	4.98	5.20	5.70	6.13	3.32
100% (1010101010101010)	8.40	8.40	6.26	6.60	7.90	8.22	4.32
Average	5.26	6.02	4.6	5.01	5.24	5.55	3.17

Table V $Delay_{C\_Q}$ in pS as a function of supply voltage

Supply Voltage (V)	PPFF	C^2MOSFF	AEFF	HPFF	Pass FF	PIFF	Proposed FF
1.0	Failed	106.90	Failed	247.65	238.15	166.35	203.32
1.2	137.85	41.35	593.20	119.95	133.60	126.65	87.32
1.3	99.99	25.61	293.43	74.31	79.77	63.78	72.44
1.4	116.40	18.25	193.65	56.35	103.55	43.52	73.17
1.6	132.40	13.35	98.25	41.25	100.30	9.90	5.11
1.8	111.75	11.55	58.40	34.05	81.30	78.61	4.22
2.0	95.30	10.30	43.75	30.30	66.15	69.54	42.07
Average (excluding 1V)	115.62	20.07	213.45	59.37	94.11	65.33	47.39

Table VI PDP_{C_Q} as a function of supply voltage

Supply Voltage (V)	PPFF	C^2MOSFF	AEFF	HPFF	Pass FF	PIFF	Proposed FF
1.0	Failed	416.91	Failed	767.72	769.22	545.63	439.17
1.2	661.68	223.29	2271.96	551.77	627.92	629.45	249.74
1.3	564.94	161.34	1467.15	389.38	440.33	378.85	244.12
1.4	756.60	135.05	1221.93	338.10	662.72	319.44	297.07
1.6	1337.24	134.84	950.08	325.88	842.52	107.91	26.27
1.8	1385.70	149.00	878.92	323.48	869.91	1072.24	27.51
2.0	1467.62	155.53	975.63	348.45	912.87	1211.39	323.52
Average (excluding 1V)	1028.96	159.84	1294.28	379.51	726.05	619.88	194.70

Table VII Transistor count of discussed flip-flops

Flip Flop	PPFF	C^2MOS FF	AEFF	HPFF	Pass FF	PIFF	Proposed FF
Number of Transistors	16	20	10	9	10	12	12
Number of Clocked Transistors	6	8	4	5	4	6	4